ABSTRACT OF THE DISCLOSURE

There is disclosed a semiconductor integrated circuit device comprising a memory cell array including a memory cell having a ferroelectric capacitor having first and second electrodes. A first bit line is electrically connected to the first electrode. A first potential generation circuit supplies a first potential to the second electrode to apply a voltage which drops at a first rate of change with a rise of temperature to the ferroelectric capacitor. A sense amplifier amplifies a potential difference between the first bit line and a second bit line complementary to the first bit line.